REMARKS

Rejection Under 35 U.S.C. §102(a)

Claims 1 -15 were rejected under 35 U.S.C. 102(a) as being unpatentable over National Semiconductor, LM2637 "Motherboard Power Supply Solution with a 5-Bit Programmable Switching Controller and Twol Linear Regulator Controllers". Rejections under 35 U.S.C. 102(a) require the disclosure in a single art reference each limitation of a claim in question.

Claims 1, 6, 11

With regards to Claim 1, Claim 1 is patentably distinguishable from the *National LM2637* reference. In particular the *National LM2637* reference does not disclose or teach a "means for delaying connection of the primary and secondary power voltages to the controlled voltage outputs for a selected delay time after the primary power voltage reaches the reference threshold level" as is disclosed and claimed in Claim 1 of the present application. Referring to page 4, lines 27 –30 and Claim 1 of the present application, the secondary voltage is not measured. One of the benefits of the present invention is that only the primary voltage is measured. As stated on Page 4, line 27-28 of the present application, "[I]t is not necessary to actually monitor the 5 and 3.3 voltages because they are related to the 12 volt supply. Instead, one monitors the 12 volt supply for overall compliance." The *National LM2637* reference teaches away from the present invention by checking all the output voltages after the soft start is completed. As stated on Page 9, column 2, Paragraph 6 of the *National LM2637* reference, "[A]t the completion of soft start, all three output voltages are checked....' This prior art method with its limitations is discussed in the Background section of the present application on page 2, lines 24-28 and the present invention is further distinguished from this prior art on page 3, lines 6-8. Accordingly, Claim 1 is patentably distinguishable from the *National LM2637* reference.

Applicant thus respectfully requests reconsideration and withdrawal of the rejection of Claim 1 under 35 U.S.C. 102(a) and allowance of said claim. Moreover, since claims 2-5 depend from and further define patently distinct Claim 1, these claims are also believed to be allowable.

With regards to Claim 6, a similar argument as the above argument with regards to Claim 1 applies. The *National LM2637* reference does not disclose or teach a computers system with monitored power that has a means to delay "connection of the controlled power output voltage to the computer for a selected delay time after the primary power voltage reaches the reference threshold level" as is disclosed and claimed in Claim 6 of the present application. The *National LM2637* reference teaches away from Claim 6 by going through a soft start procedure then monitoring all output voltages to ensure they are each within a specified range. Accordingly, Claim 6 is patentably distinguishable from the *National LM2637* reference.

Applicant thus respectfully requests reconsideration and withdrawal of the rejection of Claim 6 under 35 U.S.C. 102(a) and allowance of said claim. Moreover, since claims 7-10 depend from and further define patentably distinct Claim 6, these claims are also believed to be allowable.

With regards to Claim 11, a similar argument as the above arguments with regards to Claims 1 and 6 apply. The *National LM2637* reference does not disclose or teach "delaying connection of the power supply controlled voltage power outputs for a selected delay time after the primary power output voltage reaches the reference threshold level" as is disclosed and claimed in Claim 11 of the present application. The *National LM2637* reference teaches away from Claim 11 by going through a soft start procedure then monitoring all output voltages to ensure they are each within a specified range. Accordingly, Claim 11 is patentably distinguishable from the *National LM2637* reference.

Applicant thus respectfully requests reconsideration and withdrawal of the rejection of Claim 11 under 35 U.S.C. 102(a) and allowance of said claim. Moreover, since claims 12-15 depend from and further define patently distinct Claim 11, these claims are also believed to be allowable.

Claim 16

In regards to new Claim 16, a similar argument as the above arguments with regards to Claims 1, 6 and 11 apply. The *National LM2637* reference does not disclose or teach "a time delay circuit adapted to output the one or more secondary voltages after a select period of time

once the primary voltage equals or exceeds the reference voltage" as is disclosed and claimed in Claim 16 of the present application. Moreover, the *National LM2637* reference teaches away from Claim 16 by going through a soft start procedure then monitoring all output voltages to ensure they are each within a specified range. Accordingly, Claim 16 is patentably distinguishable from the *National LM2637* reference.

Claim 21

In regards to new Claim 21, a similar argument as the above arguments with regards to Claims 1, 6, 11 and 16 apply. The *National LM2637* reference does not disclose or teach a "time delay circuit adapted to delay the coupling of the two or more voltages to the outputs for a select period of time after the comparator has sensed the one voltage received on the first input equals or exceeds the reference voltage" as is disclosed and claimed in Claim 21 of the present application. Moreover, the *National LM2637* reference teaches away from Claim 21 by going through a soft start procedure then monitoring all output voltages to ensure they are each within a specified range. Accordingly, Claim 21 is patentably distinguishable from the *National LM2637* reference.

CONCLUSION

Claims 6, 7 and 11 are amended and claims 16-25 are added; as a result, claims 1-25 are now pending in this application. Applicant respectfully submits that the claims 1-25 are in condition for allowance and notification to that effect is earnestly requested. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2206.

If necessary, please charge and additional fees or credit overpayment to Deposit Account No. 501373.

Respectfully submitted,

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MARKED UP VERSION SHOWING CHANGES MADE

IN THE CLAIMS

6. (Amended Once) A computer system with monitored power comprising in combination:

a power supply for generating a primary dc power voltage and one or more secondary dc power voltages [voltags] derived from the primary dc power output, a motherboard comprising multiple units including a memory unit and a central processing unit, wherein said units [uits] may require different operating voltages; and a power monitoring integrated circuit disposed between the power supply and the motherboard for controlling supply power from the power supply to the mother board, said power monitoring circuit comprising,

input means for receiving the primary and secondary power voltages from the power supply;

means for controlling the received [receviced] power voltages to generate controlled voltage power outputs;

means for comparing a signal representative of the primary power voltage to a reference signal;

means for sensing when the primary power voltage reaches or exceeds a threshold reference level; and

means for delaying connection of the controlled power output voltages to the computer for a selected delay time after the primary power voltage reaches the reference threshold level.

7. (Amended Once) The computer system of claim 6 further comprising means for generating a power up signal for indicating that all the monitored output voltages of the monitored power supply are at or above a usable and effective voltage level.

11. (Amended Once) A method for monitoring and controlling power from a power supply that generates a primary power voltage and one or more secondary power voltages derived from the primary power voltage, comprising:

receiving the primary and secondary power voltages from the power supply;

controlling the received power voltages to generate controlled voltage power outputs;

comparing a signal representative of the primary power voltage to a reference signal;

sensing when the primary power output voltage reaches or exceeds a threshold reference level; and

delaying connection of the power supply controlled [contolled] voltage power outputs for a selected delay time after the [input power supply] primary power output voltage reaches the reference threshold level.

16. (New) A power monitor circuit comprising:

a primary input adapted to receive a primary voltage from a power supply;

one or more secondary inputs to receive one or more secondary voltages from the power supply, wherein the one or more secondary voltages are derived from the primary voltage;

a comparator circuit adapted to compare the primary voltage with a reference voltage; and

a time delay circuit adapted to delay an output of the one or more secondary voltages after a select period of time once the primary voltage equals or exceeds the reference voltage.

17. (New) The power monitor circuit of claim 16, wherein the comparator circuit further comprises:

a resistor divider network adapted to divide the primary voltage, the resistor divider network comprising:

a first resistor of a first select value, and

a second resistor of a second select value, the first and second resistor being adapted to divide the primary voltage into a select divided primary voltage; and

a comparator having a first input coupled to the resister divider network to receive the select divided primary voltage, the comparator having a second input coupled to receive the reference voltage, the comparator further having an output coupled to the time delay circuit.

18. (New) The power monitor circuit of claim16, wherein the reference voltage is approximately equal to 90% of the primary voltage.

19. (New) The power monitor circuit of claim 16, wherein the time delay circuit outputs the primary and one or more secondary voltages approximately 40ms after the primary voltage equals or exceeds the reference voltage.

20. (New) The power monitor circuit of claim 16, wherein the primary voltage is approximately equal to 12 volts, one of the secondary voltages is approximately equal to 3.3 volts and another of the secondary voltages is approximately equal to 5 volts.

21. (New) A power monitor circuit for monitoring two or more voltages from a power supply wherein the power supply derives the two or more voltages from a single voltage, the power monitor circuit comprising:

a first input adapted to receive one voltage of the two or more voltages from the power supply;

a secondary input for each of the remaining two or more voltages, each secondary input adapted to receive an associated one of the remaining two or more voltages;

an output for each of the two or more voltages;

a comparator circuit adapted to compare the one voltage received at the first input with a reference voltage; and

a time delay circuit adapted to delay the coupling of the two or more voltages to the outputs for a select period of time after the comparator has sensed the one voltage received on the first input equals or exceeds the reference voltage.

22. (New) The power monitor circuit of claim 21, wherein the one voltage received on the first input is a primary voltage and the remaining two or more voltages are secondary voltages derived from the primary voltage.

23. (New) The power monitor circuit of claim 21, wherein the reference voltage is in relation to 90% of the nominal setting of the one voltage received at the first input.

24. (New) The power monitor circuit of claim 21, wherein the select period of time is approximately 40ms.

25. (New) The power monitor circuit of claim 21, further comprising:

a voltage divider adapted to divide the one voltage received on the first input, wherein the divided one voltage received on the first input is compared to the reference voltage.